International Journal of Electronics, Communication & Instrumentation Engineering Research and Development (IJECIERD)
ISSN (P): 2249-684x; ISSN (E): 2249-7951
Vol. 8, Issue 3, Aug 2018, 1-10
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DELAY EFFICIENT 128-BIT LADNER-FISCHER ADDER

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ABSTRACT

This paper describes the VLSI Architecture for High-Speed 128-bit Ladner-Fischer adder. The performance of Ladner-Fischer adder with black cell takes huge memory. So, the gray cell can be replaced instead of black cell that improves the Efficiency in Ladner-Fischer Adder. The three stages of operations include pre-processing stage, carry generation stage, post-processing stage. In ripple carry, adder each bit of addition need to wait for the previous bit carry. In efficient Ladner - Fischer adder, addition operation does not wait for previous bit carry since ripple carry adders are replaced by Carry select Adder (CSLA) and Binary to Excess-1 code Converter (BEC) to improve the speed and to decrease the memory used.

KEYWORDS: Ladner-Fischer Adder, Ripple Carry Adder (RCA), Carry Select Adder (CSLA), Binary to Excess-1 Code Converter (BEC-1), Black Cell & Gray Cell

Received: May 16, 2018; **Accepted**: Jun 06, 2018; **Published**: Jul 06, 2018; **Paper Id**.: IJECIERDAUG20181

Original Article 1

INTRODUCTION

The digital circuit used for addition of numbers is termed as Adder. The speed and efficiency of a processor or system depend on the type of adder used in the system. In most of the Digital signal processing processors, the addition operation is performed using a simple ripple carry adder. The most commonly used adders are a half adder and the Full adder.

Half adder is used for the addition of two bits results in sum with a delay of 3units and carry of 1 unit delay. Full adder is utilized for the addition of three bits which results in sum with delay of 6 units and carry of 5 units delay. A Ripple carry adder is a logical circuit created by using multiple full adders.

In this paper, 128bit proposed Ladner-Fischer Adder using Carry select adder and Binary to excess-1 code converter are presented using Verilog HDL language.

The brief is structured as follows. Section II deals with Adders. Black cell, gray cell and Ladner-Fischer Adder are presented in sections III. Section IV represents proposed Ladner-Fischer adder. Sections V and VI deals with results and conclusion [6].

ADDERS

The classification of Adders includes parallel prefix adder and serial prefix adder. Parallel Prefix Adder (PPA) is fast when compared with a ripple carry adder. PPA is a family of adders is derived from carry look ahead adders. These adders are best suited for additions with wider word lengths. Different type of adders is explained below.

Ripple Carry Adder

RCA is a combination of full adder (FA) and the half adder (HA) arranged in a sequential order. In RCA carry generated in each full adder will be rippled to their next preceding full adders so the term ripple carry adder.

Generally, a 128-bit Ladner-Fischer adder requires 128-bit Ripple carry adder. A Ladner-Fischer adder uses black cells and gray cells with a combination of ripple carry adders. So in order to achieve efficient delay, these RCA adders are replaced by CSLA and BEC.

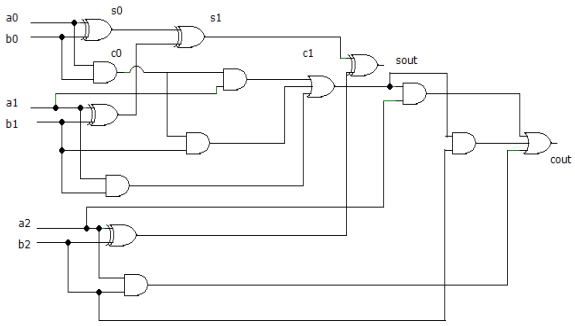

Figure 1: Ripple Carry Adder (RCA) for 3 Bit

The above diagram shows the addition of 3bits using ripple carry adder which has the delay of 10units for generation of sum and 9units for carrying.

Carry Select Adder

A Carry Select Adder is a modified RCA which consists of two ripples carry adders and multiplexer. As shown in the figure below the total number of 6bits are divided into two equal halves. The 3bits in the first half are added normally using full adders as shown in stage-1 and the bits in the second half are added by taking carry from stage-1and assumed to be 0 and 1 in stage 2 and 3 respectively. The outputs from stage 2 and 3 are generated simultaneously and the multiplexer is used to select the output with carrying from stage-1 as selection line.

Since the stage-2 and stage-3 are simultaneously generated in CSLA the delay is reduced when compared to Ripple carry adder.

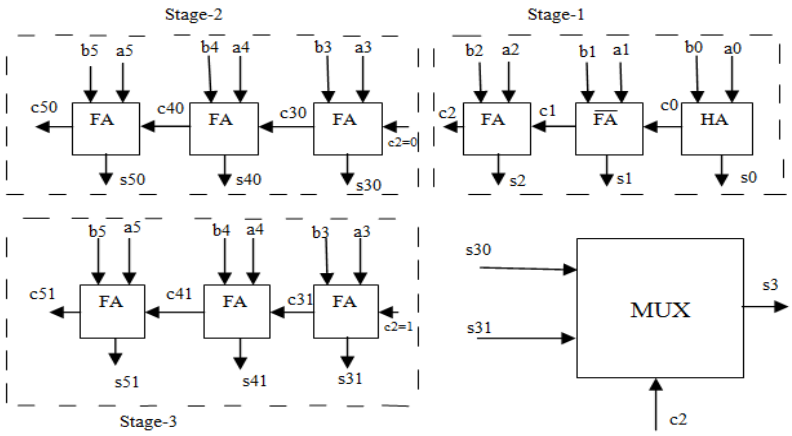

Figure 2: CSLA Used for Addition of Two 6-Bits

Binary to Excess-1 Code Converter Adder

A Binary to Excess-1 converter consists of XOR, NOT, AND gates as shown in the figure. BEC-1 is taken as a compromise between CSLA and RCA. By using BEC-1 adder efficient area and delays can be achieved. The carry=1 stage in CSLA is replaced by Binary to excess -1code converter to reduce delay and area.

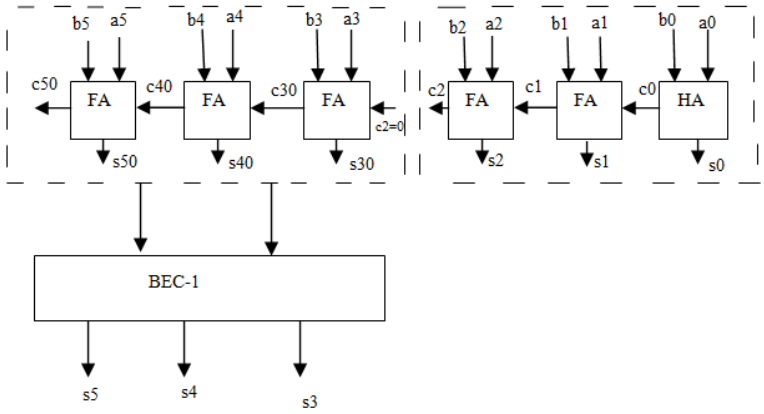

Figure 3: BEC-1 Adder Used for Addition of Two 6-Bits

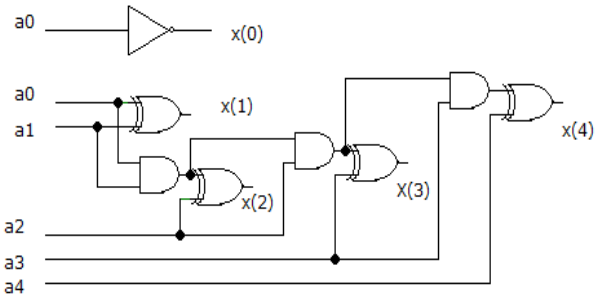

Figure 4: Binary to Excess Code Converter-1

LADNER-FISCHER ADDER

Ladner-Fischer adder is a tree-like structure that speeds up the process of addition. It is one of the parallel prefix adders. Ladner-Fischer adder consists of the black cell and Gray cell. The black cell consists of two AND gates and one OR gate. Gray cell consists of one AND and one OR gate. The Ladner-Fischer adder consists of three stages. They are a pre-processing stage, carry generation stage and post- processing stage.

In the pre-processing stage, the propagate gives “XOR” operation of input bits and generates gives “AND” operation of input bits. The propagate (Pi) and generate (Gi) are shown below

$$p_i = a_i \bar{b_i} + \bar{a_i} b_i$$

$$G_i = a_i \, and \, b_i$$

In the carry generation stage, black cells and gray cells are used according to the requirement. The carry propagate (c_p) and carry generation (c_g) is generated for black cell and carry propagate is generated for the gray cell.

$$c_p = p_1.p_0$$

$$c_g = g_1 + p_1.p_0$$

The last stage, post-processing stage the carry of a first bit is XORed with the next bit of propagates then the output is given as sum.

$$s_i = p_i xor c_{i-1}$$

Black Cell

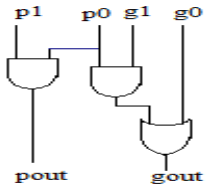

Figure 5: Black Cell

The black cell consists of four inputs (g0, p0, p1, g1) and three logic gates- two AND and one OR gate. The outputs gout and pout in the above diagram is given as inputs to the next black cell along with p2 and g2. The process is repeated until the desired output is obtained. Black cell utilizes more memory and delay. In order to reduce them, Black cell can be replaced by Gray cell.

Gray Cell

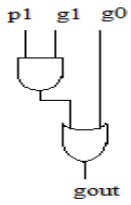

Figure 6: Gray Cell

Gray cell is a logical adder gate which contains only three inputs (g0, g1, p1). The output from the gray cell gout is given as input to the next gray cell along with p1 and g2.

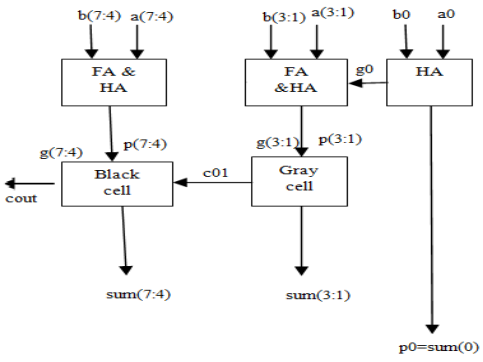

Figure 7: Ladner-Fischer Adder for 8bit with Black & Gray Cell

The figure 7 shows the block diagram of a ladner-Fischer adder for 8bit using both black and gray cells.

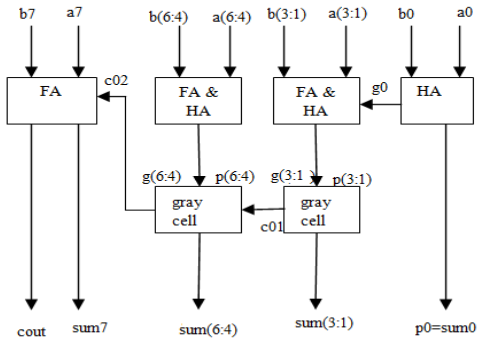

Figure 8: Ladner-Fischer Adder for 8bit using Gray Cell

The above figure shows the block diagram of Ladner-Fischer adder for 8bit using only gray cells which reduces the delay and memory when compared to Ladner-Fischer adder with black and gray cells.

Proposed Architecture for Ladner-Fischer Adder

In the proposed Ladner-Fischer adder the adders which uses black cell need not wait for the carry from the gray cell. The carry from the gray cell is assumed as 0 and 1 and the addition operation simultaneously takes place.

The result from both cases is selected by using a multiplexer (2:1) which contain two inputs, one from 0 cases and the other from 1 case. The selection line used for selection of desired output is the carry generated from the gray cell which was assumed as 0 and 1 mentioned before.

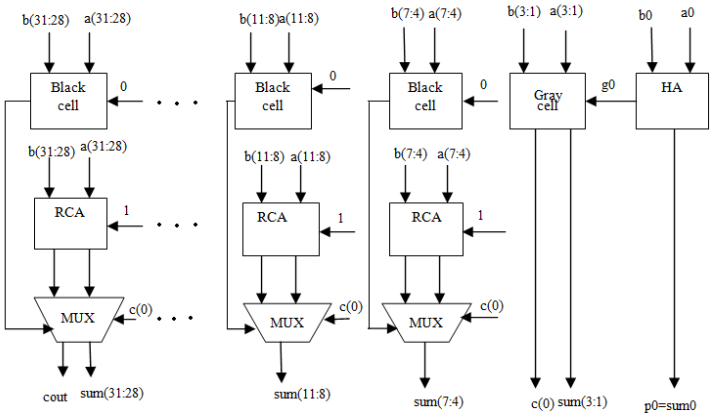

Figure 9: Linear CSLA Ladner-Fischer Adder for 32 Bit

By using CSLA in the place of ripple carry adders the delay can be greatly reduced but the memory is increased since the utilization of logic gates has increased. In order to decrease the memory used CSLA is replaced by BEC adder as shown below.

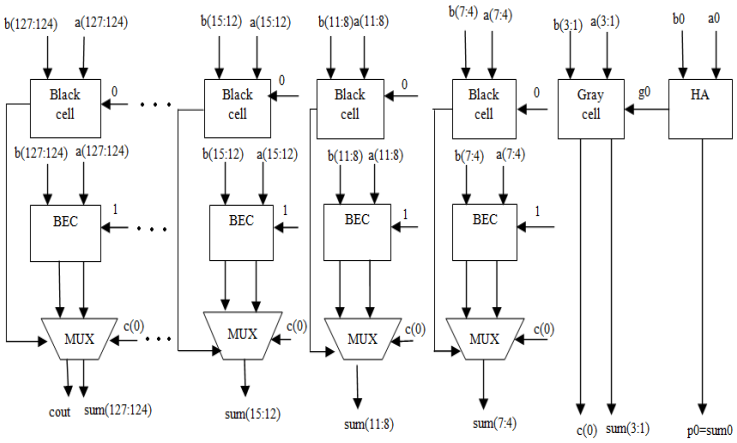

Figure 10: Ladner-Fischer Adder using BEC for 128 Bit

The above figure shows the block diagram for 128bit Ladner-Fischer adder using BEC. Binary to Excess-1 code converter is a trade-off between the normal Ladner-Fischer adder and Ladner-Fischer using CSLA.

RESULTS

The simulation results for Ladner-Fischer adder using XILINX software are shown.

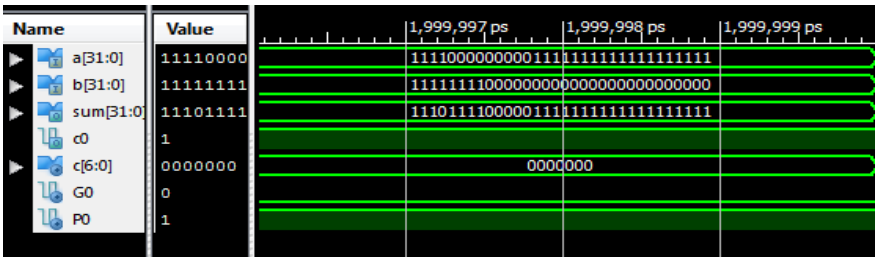

Figure 11: Simulation Results for 32 Bit Ladner-Fischer Adder using Black and Gray Cell

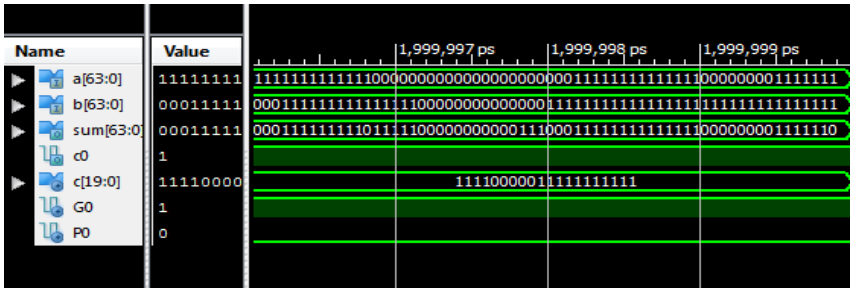

Figure 12: Simulation Results for 64 Bit Ladner-Fischer Adder using Gray Cell

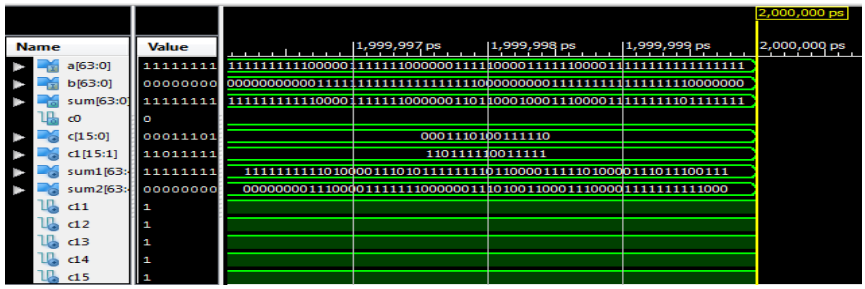

Figure 13: Simulation Results for 64 Bit Ladner-Fischer Adder using Carry Select Adder(CSLA)

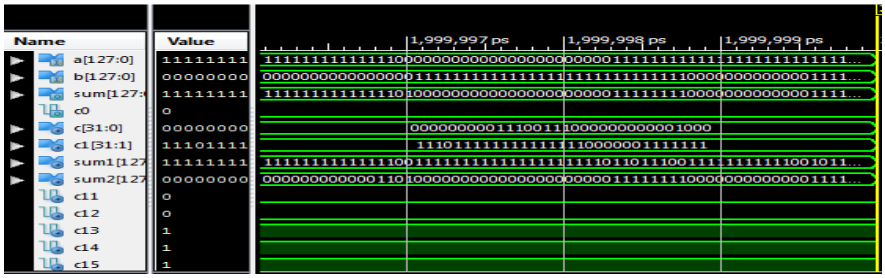

Figure 14: Simulation Results for 128 Bit Ladner-Fischer Adder using Binary to Excess-1 Code Converter (BEC)

A graph is plotted for the delay in nanoseconds for 128bit Ladner-Fischer adder using Black cell and Gray cell, only gray cell, using CSLA and using BEC and figure14 shows the memory Utilization of 64bit Ladner-Fischer adder.

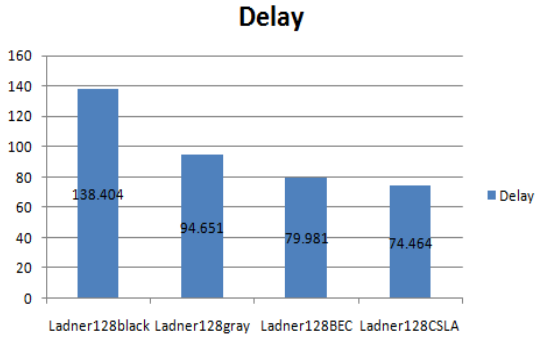

Figure 15: Delay Comparison for 128-Bit Ladner-Fischer Adder

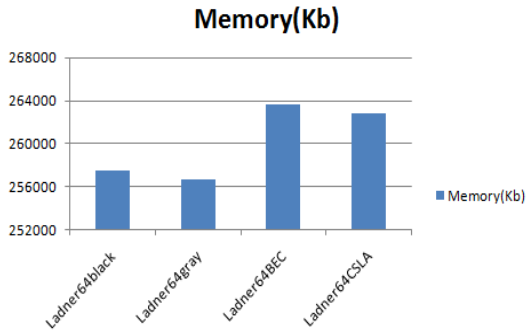

Figure 16: Memory Utilization of 64 Bit Ladner-Fischer Adder

Utilization Summary

The table1, table2 and table3 shows device utilization of the Ladner-Fischer adder using RCA, CSLA and BEC-1 for 16bit, 32bit, 64bit and 128bit

Table 1: Ladner-Fischer Adder Device Utilization

Device Utilization	Ladner 16bit	Ladner 32bit	Ladner 64bit	Ladner 128bit
No. of slice Registers	19	37	74	147
No. of IOBs	49	97	195	385
Memory in KB	253104	255088	257456	264112
Delay in ns	19.578	36.553	70.503	138.404
No. of 4 input LUT's	33	65	130	257

Table 2: Comparison Between Ladner-Fischer Adder with RCA, BEC-1 and CSLA Adders for 64 Bit

Device Utilization	Ladner64 RCA	Ladner64CSLA	Ladner64 BEC
No. of slice Registers	74	104	104
No. of IOBs	195	193	193
No.of4 input LUTS	130	174	186
Memory in KB	257456	263600	262768
Delay in ns	70.503	39.618	43.421

Table 3: Comparison Between Ladner-Fischer Adder with RCA, BEC-1 and CSLA Adders for 128 Bit

Device Utilization	Ladner128 RCA	Ladner128 CSLA	Ladner128 BEC
No. of slice Registers	147	194	214
No. of IOBs	385	385	385
No.of4 input LUTS	257	355	383
Memory in KB	264112	277232	276208
Delay in ns	138.404	74.464	79.981

CONCLUSIONS

From the tables, it is clear that delay for 128bit Ladner-Fischer adder using CSLA(74.464) is less when compared to the delay of Ladner-Fischer adder using RCA(138.404).

Ladner-Fischer adder using BEC is a compromise between Ladner-Fischer adder using RCA and CSLA. By using CSLA memory is increased as shown in the table. To reduce the memory is the requirement for the system Ladner with RCA can be used. If reduction of delay is a major requirement then Ladner with CSLA can be used. If both memory and delay are requirements then Ladner with BEC can be used in the system.

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